ENCQOR 5G Academic Technology Development Program Challenge Statement

Title: **FPGA based Virtual Fabric for Distributed FOG/Edge Computing**

Challenge Launch Date	• July 3, 2019
Challenge Deadline	• July 31, 2019
Challenge Statement	5G and IoT infrastructure and new applications are expected to generate massive amounts of data, thereby driving changes to network architecture. Data processing and content distribution will be forced closer to the network edge, driving the need for much more efficient and programmable edge compute infrastructure. Traditionally, such edge compute infrastructure needs have been met with Field Programmable Gate Arrays (FPGAs) providing a reprogrammable protocol handling layer (at PHYs or NICs), and generic CPUs (possibly augmented with GPUs) interconnected through a largely static network switching fabric. The objective of this project is to investigate approaches and develop a software tool kit for managing and programming a fabric of interconnected FPGAs. The FPGA fabric (i.e. multiple FPGAs interconnected to appear as a single large virtual FPGA) is intended to absorb functions that are currently spread across multiple elements: protocol adapters, switching ASICs, networking functions, data processing CPU/GPU functions, etc. The project is expected todeliver a set of algorithms, techniques and tools for adaptive and optimized sizing, placement and chaining of required functions inside the FPGA fabric.
Project Partner	Ciena
Timeline	2 years
Available funding	Up to $150 000 CDN
Applicant Type	Ontario based College/University
Location	Work can be completed at the applicant institution. Some travel to Ciena's facilities in Kanata, Ontario may be required

Project Details	For this project Ciena is interested in considering a new architecture for an FPGA based virtualized and programmable infrastructure for efficient data processing, with a focus on edge data centers. The primary application is at the network edge, where end user traffic is aggregated and processed before being transported into the core network and centralized data centers. The same approach could also be used in the centralized data centers, as well as in Access WAN network design. FPGAs are known to provide substantial throughput, power performance, and application design flexibility benefits over CPUs and GPUs for a number of workload types including: protocol adapters, AI training and inference, deep packet inspection and parsing, and machine learning. An FPGA based virtualised and programable infratsturutre is anticipated to have the following attributes: • A Flat, scalable "compound graph" interconnecting multiple FPGAs to provide an efficient, low diameter network to minimize data traversal across expensive links. • Data processing functions will be absorbed into the FPGAs minimizing the use of traditional CPU/GPU resources. • Switching functionality is completely pulled into FPGA-based fabric (via Open vSwitch, P4, etc) -- a separate Leaf/Spine network switching layer is eliminated. • Processor functions migrate from CPUs into the FPGA layer. • The architecture should enables global optimization for data ingestion from physical interfaces, data routing and processing and network function placement. The project is likely to use commercial off-the-shelf multi-FPGA hardware for the development of a prototype. However, the development of concepts for improved FPGA interconnection is within project scope. The main focus of the research project will be software. The software design and development should reuse applicable open source code, and address the following: • Software toolkits for developing Switching and Processing Virtual networking Functions (VNFs) amenable to be placed onto a distributed FPGA substrate • Development of individual functional blocks, including physical interfaces, as well as Switching and Processing VNFs. • Algorithms for optimal sizing, placement and chaining of Switching and Processing VNFs • Methods and tools for hitless deployment and maintenance of Switching and Processing VNFs

	Some examples of existing multi-FPGA tools and open source projects are below. These are provided as examples only and are not intended to be exhaustive or suggestive of a particular approach or solution: • http://www.s2cinc.com/products/prodigy-player-pro • http://asim.csail.mit.edu/redmine/projects/ • https://www.cs.cornell.edu/~jnfoster/papers/p4fpga.pdf • https://elinux.org/images/7/79/Open-Source_Tools_for_FPGA_Development.pdf
Project Goals/ Outcomes	A working prototype of the FPGA fabric with a corresponding set of software configuration and management tools to demonstrate a basic functionality of a programmable, adaptive and optimized FPGA fabric.
Applicant Capabilities	PhD Candidate(s) capabilities: • Minimum of 1 and preferably 2 candidates available to perform the research • Students should have familiarity with networking concepts • Students should be able to independently use FPGA programming packages to develop and refine resource optimization and placement approaches • Students should be comfortable with performing independent research on existing academic and industrial work in the area of FPGA virtualization • Students should have working experience with a set of programming languages that may be used in the project (C/C++, Python, etc.) Applciant Principal investigator(s) capabilities: • Comprehensive understanding and working experience with FPGA programming tools • Familiarity with commercial tools used for mult-FPGA optimization • Familiarity with academic research and open source projects that address different aspects of FPGA-based programmable infrastructure
Additional Information	• Applicants should be able to assign any intellectual property discovered during this project to Ciena. • Given the scale of the research project it is anticipated that the project may result in opportunities for conferences and journal publications.

Launched in 2018, the ENCQOR 5G Academic Technology Development Program partners Ontario based Researchers with ENCQOR 5G Anchor Firms on 5G technology development projects. Areas of research interest are defined by Challenge Statements submitted to OCE by the ENCQOR 5G Anchor Firms and posted to the OCE website on a rolling basis.

If you are interested in developing an expression of interest, please visit the program guidelines for information on next steps.

For any questions about new Challenge Statements or the ENCQOR 5G SME Technology Development Program please contact Sarah Fairlie at sarah.fairlie@oce-ontario.org'